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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 04/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/716,259	RAMESH ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *29 and 30* is/are allowed.

6)☒ Claim(s) *1-5 and 16-19* is/are rejected.

7)☒ Claim(s) *6-15 and 20-28* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are presented for examination.

Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1, 16, 29-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims1, 16, the phrase "or " renders the claim(s) indefinite because the claim(s) include(s) elements not actually disclosed (those encompassed by "or "), thereby rendering the scope of the claim(s) unascertainable. See MPEP § 2173.05(d).

In claims 1, 16, applicant discloses a shared contact structure is formed "**I)**" and "**ii)**" **or** "**iii)**". It does not clearly to point out subject matter which applicant regards as the invention.

Claims must be amended for more clearly as request.

Regarding claims 29-30, claim disclosed "a second metal layer" and "a third metal layer". However, a first metal layer does not disclose. When number is used for naming of element. The number should be used in order. For example, before a second layer must have first metal layer...etc..

Regarding claim 29, claim disclosed "one **or** more subsystems" is not clear to point out which applicant regarding as the invention as defined above.

Claims 29-30 should be amended for more clearly as described above.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim1 is rejected under 35 U.S.C. 102(b) as being anticipated by Higashide (U.S. Patent No. 6,222,758).

Regarding claim 1, Higashide discloses a memory array comprising a plurality of memory cells arranged in one or more rows and columns (Column 1, lines 21-47), wherein each memory cell shares at least one contact structure with a vertically adjacent memory cell (Column 13, lines 1-15), wherein the shared contact structure is formed proximate to a boundary between the memory cell and the vertically adjacent memory cell (column 3, lines 1-15,Column 4, lines 14-25), such that the shared contact structure is formed: i) completely within the memory cell on one side of the boundary ii)

completely within the second memory cell on an opposite side of the boundary (Column 6, lines 20-43), or iii) formed at the boundary, such that unequal portions of the shared contact structure are formed on either side of the boundary.

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 1-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Ishiguro (U.S. Patent No. 6,947,577).

Regarding claim 1, Ishiguro discloses a memory array comprising a plurality of memory cells arranged in one or more rows and columns (Figure 1), wherein each memory cell shares at least one contact structure with a vertically adjacent memory cell (Column 1, lines 13-32), wherein the shared contact structure is formed proximate to a boundary between the memory cell and the vertically adjacent memory cell (Column 2, lines 9-25), such that the shared contact structure is formed: i) completely within the memory cell on one side of the boundary ii) completely within the second memory cell on an opposite side of the boundary (Column 2, lines 1-25, or iii) formed at the

boundary, such that unequal portions of the shared contact structure are formed on either side of the boundary.

Regarding claims 2-5, Ishiguro discloses wherein the shared contact structure is configured for coupling an overlying bit line to an underlying diffusion region (Column 12, lines 48-67, column 14, lines 1-5), and wherein the shared contact structure is configured for coupling an overlying ground supply line to an underlying diffusion region (column 13, lines 59-67), and wherein the shared contact structure is configured for coupling an overlying power supply line to an underlying diffusion region (Column 13, lines 59-67, column 14, lines 15-25), and wherein a length of the memory array is reduced by sharing the contact structure between the memory cell and the vertically adjacent memory cell (Column 5, lines 10-15) .

8. Claims 16-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Castagnetti et al. (U.S. Patent No. 6,778,462).

Regarding claim 16, Castagnetti et al. disclose a dual-port memory cell (Figure 2, 200), comprising:

a first pair of N-channel access transistors (Q5, Q6) coupled through respective gate terminals by a first local word line (WLA) of the memory cell;

a second pair of N-channel access transistors (Q7, Q8) coupled through respective gate terminals by separate portions of a second local word line (WLB) of the memory cell; and

a plurality of bitline (BLA, BLB, /BLA, /BLB) contact structures coupled to drain terminals of the first and second pairs of access transistors and to drain terminals of corresponding pairs of access transistors arranged within a vertically adjacent memory cell, wherein the bitline contact structures are formed i) completely within the memory cell, ii) completely within the adjacent memory cell (Figure 5), or iii) having unequal portions within the memory cell and the adjacent memory cell.

Regarding claims 17-19, Castagnetti et al. disclose first and second inverter circuits (Figure 2), each including a P-channel latch transistor (Q1, Q2) coupled in common- gate configuration with an N-channel latch transistor (Q3, Q4) , wherein drain terminals of the P- channel and N-channel latch transistors are coupled to respective source terminals of the first and second pairs of N-channel access transistors (Figures 2,5). More specifically, Castagnetti et al. disclose a pair of power supply (Figure 5, Vdd, Vss) contact structures coupled to source terminals of the P-channel latch transistors and a pair of ground supply contact structures coupled to source terminals of the N-channel latch transistors, wherein the pairs of power and ground supply contact structure s are shared between the memory cell and the adjacent memory cell, such that one power supply contact structure and one ground supply contact structure are arranged within each of the memory cells (Figure 5), and wherein the access transistors and the latch transistors are formed, such that source/drain current flows through the access and latch transistors along a length of the memory cell (Figure 5).

Allowable Subject Matter

9. Claims 6-15, 20-28 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 6-15, 20-28 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Higashide (U.S. Patent No. 6222,758), Ishiguro (U.S. Patent No. 6,847,577), Castagnetti et al. (U.S. Patent No. 6,778,462) and others, does not teach the claimed invention having a column of memory cells is formed by rotating vertically adjacent memory cells about an x-axis and a y-axis, wherein the x- and y-axes extend horizontally and vertically, respectively, through a center of each memory cell as claims 6-15 disclose, and a first metal layer dielectrically spaced above and coupled to the access transistor and latch transistor through corresponding contact structures as claims 20-28 disclose.

10. Claims 29-30 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

Claims 29-30 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Higashide (U.S. Patent No. 6222,758), Ishiguro (U.S. Patent No. 6,847,577), Castagnetti et al. (U.S. Patent No. 6,778,462) and others, does not teach the claimed invention having a one or subsystems coupled to the memory array through

a fourth metal layer arranged above the third metal layer, wherein the fourth metal layer comprises a plurality of transmission lines.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Le

Thong Q. Le
Primary Examiner
Art Unit 2827

THONG LE
PRIMARY EXAMINER